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An Analysis Method of System-Level ESD Model with a TLP Stress Input

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Abstract Based on the existing equivalent formula of the transmission line pulse (TLP) and IEC 61000-4-2 stresses, the authors propose an analysis method of the system-level model with TLP stress as an input. Compared with the traditional analysis method under system-level IEC stress, the proposed method solves the issue that the calculation of the residual energy flowing into the device under test (DUT) is not accurate enough. Meanwhile, the prediction ability for the failure of the DUT is promoted. This work predicts the failure of the DUT under the mentioned two stresses through SPICE simulation. Furthermore, this work shows the validation through the measured results of the relevant printed circuit boards (PCBs), which confirms the promotion of the aforesaid prediction ability.

Key words electro-static discharge (ESD); transmission line pulse (TLP) test; ESD gun; residual energy

一种基于 TLP 输入的系统级 ESD 模型分析方法

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摘要 基于已有的传输线脉冲发生器(TLP)与 IEC 61000-4-2 应力的等效关系, 提出一种以 TLP 应力作为输入的系统级模型分析方法。与传统的 IEC 应力作为系统输入的分析方法相比, 该方法解决了对流入待测器件(DUT)残余能量的计算不够精确的问题, 同时提高了 DUT 失效预测方面的精准性。通过 SPICE 仿真, 预测了上述两种应力作为系统输入的 DUT 失效情况。通过相应的印制电路板(PCB)的实测验证, 进一步说明新提出的方法能够提高系统级失效预测的精准性。

关键词 静电放电; 传输线脉冲测试; 静电枪; 残余能量
中图分类号 TP333

Electro-static discharge (ESD) protection design for the device under test (DUT) to survive the system-level stress prescribed in IEC 61000-4-2 standard is important[1]. Compared with the traditional trial-and-error method, an efficient design method is to build the models of system-level ESD protection circuits to save time and cost[2–6]. Fig. 1 shows a system-level circuit model where the isolation network and transient voltage suppressor (TVS) protect the DUT from being damaged by the IEC ESD stress[7]. Although the TVS and isolation network resist the main IEC energy, there is still the residual energy flowing into the DUT.

As for the DUT, the robustness can be addressed by the transmission line pulse (TLP) test. Meanwhile, the failure current I_{t2} of the DUT under TLP test is

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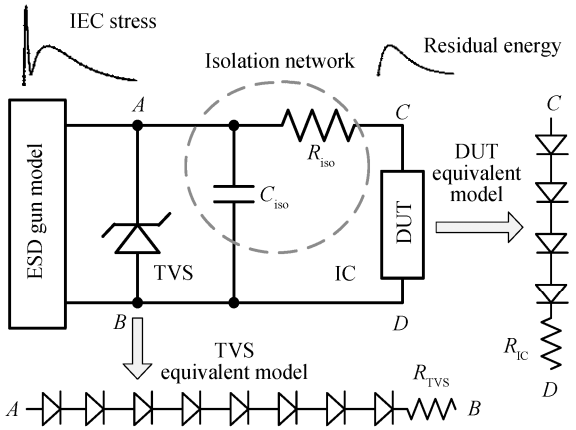

Fig. 1 A previous system-level ESD protection circuit model

adopted as a system-level failure standard[7]. In fact, a TLP tester generates a DC square wave, but the real residual energy of the IEC stress is not the square wave as shown in Fig. 1. Although the two kinds of stresses have almost the same time width, it is not accurate using the above mentioned I_{t2} to stand for the marginal failure value of the DUT under the residual energy. This work proposes a system-level model with TLP stress as an equivalent input of IEC stress so that the shape of the residual energy is a square wave. Therefore, the I_{t2} under the TLP test can be regarded as the failure standard of the DUT in system-level.

1 System-level Model with TLP as Input

Fig. 2 shows the system-level model with the TLP stress as an equivalent input of the IEC stress. As for the TLP model, two relay switches control the charging and discharging of a transmission line T_{original} with 50-ns delay to deliver a 100-ns TLP stress. The transmission line T_{con} is used to connect the TLP tester and DUT. The characteristic impedance Z_0 of T_{original} is 50 Ω and it is the same with T_{con}, so the TLP current can be calculated by a pre-charge voltage V_1/50 in short state of DUT. During the modeling process, the DUT is regarded as a black box and it is measured to obtain *I*–*V* and transient curves under the TLP test. Furthermore, the model of the DUT can be built based on the measured curves. Fig. 2 also shows the TVS and DUT models in detail.

Taking an example of the TVS, *V* stands for the breakdown voltage measured in the relevant *I*–*V* curve. R_{TVS} stands for the on resistance and a voltage controlled resistor *S* decides whether the TVS is in open state under the TLP or IEC stress. Fig. 3 (a) shows the comparison of the TVS between simulated and measured *I*–*V* curves under TLP stress and Fig. 3 (b) shows the relevant comparison of the DUT. Obviously, the results show that the TVS and DUT model are accurate. In addition, the failure current I_{t2} of the DUT under TLP test are also shown in Fig. 3 whose value is 3.3 A. In order to increase the accuracy of the models, compared with the traditional models in Fig.1, this work adds the transient analysis for the proposed component models in addition to matching the measured *I*–*V* curves. Taking the TVS model as an example, the transient curves are measured under TLP stress with 10-V step-size from 10 to 50 V. Using the above-mentioned TLP and TVS models, the relevant transient current curves can be simulated and the compared results with measured ones are shown in Fig. 4. At the beginning of transient curves in Fig. 4, the “steps” or overshoots are observed and they are the incident pulses caused by T_{con} of the TLP tester. Moreover, at the range of time from 10 to100 ns, the amplitudes of the transient curves are not constant at first and the reason is the charging of the parasitic capacitor C_{par} of the TVS. When delivering a TLP stress into the TVS, the stress will charge the C_{par} of the TVS at first. Then the TVS will turn on once the

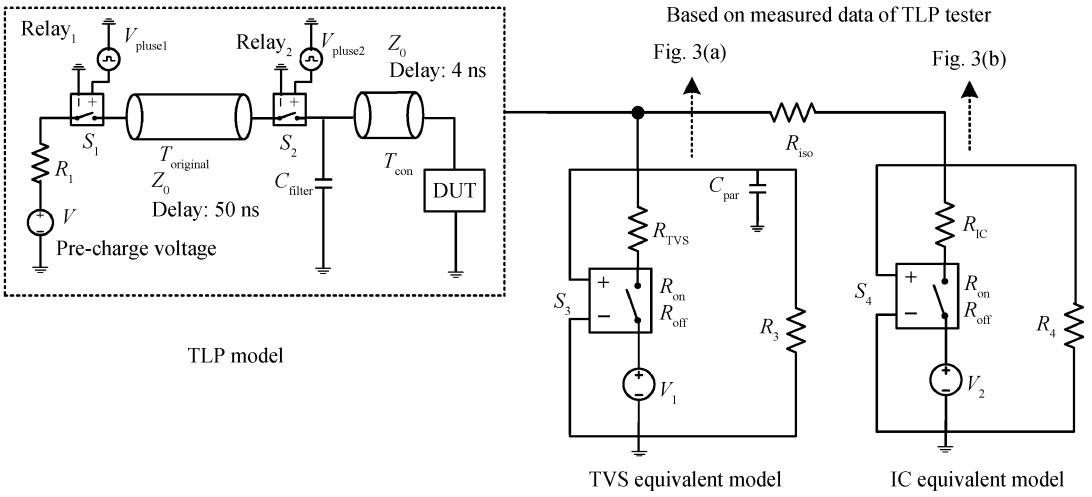

Fig. 2　Proposed circuit model with TLP stress as an equivalent input of the IEC one

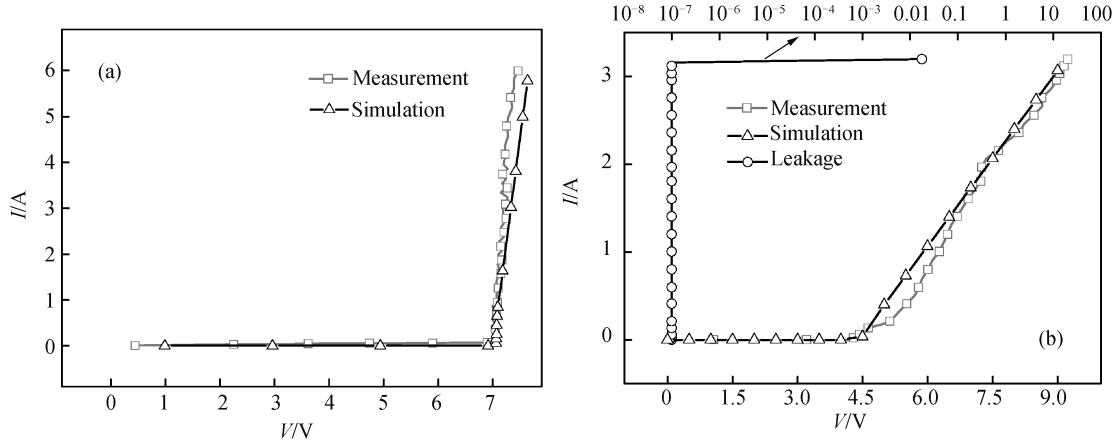

Fig. 3　Comparison of the TVS between simulated and measured *I*–*V* curves under TLP stress (a) and the comparison of the DUT (b)

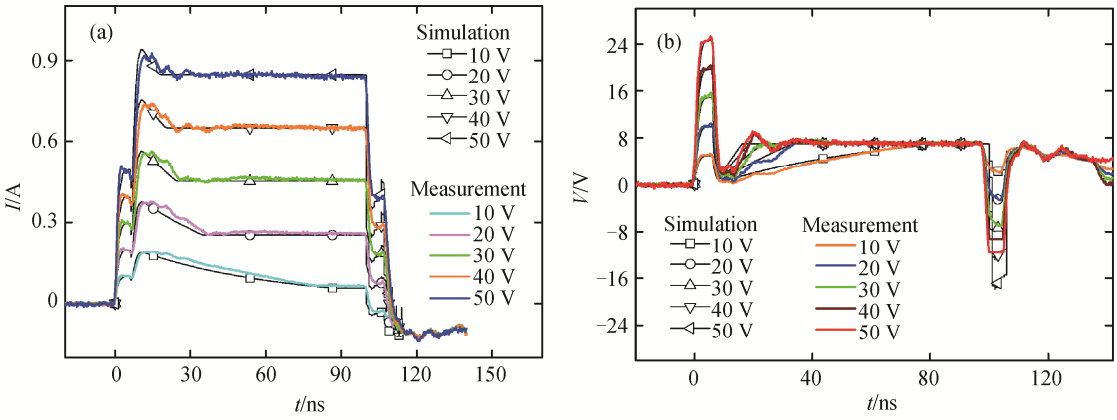

Fig. 4　Comparison of the TVS between simulated and measured transient current curves (a) and transient voltage ones (b)

voltage at both ends of the C_{par} reaches to 7-V clamping voltage of TVS. With the increasing of the TLP stress, the charging speed for the C_{par} is also improved and the relevant charging time is shorten which is can be obviously observed in Fig. 4.

As for the system-level model with TLP as an input, when the TLP current is increasing, the energy of the TLP stress flowing into the system is also increasing as well as the residual energy flowing into the DUT. From Fig. 5, it can be seen that the residual energy flowing into the DUT is a 100-ns square wave. Thus, it is accurate that taking the aforesaid 3.3-A I_{t2} under 100-ns TLP test as the failure standard of the DUT in system-level, because TLP input stress and the residual energy are both square waves. If the residual energy of TLP stress is beyond the above I_{t2}, it means the failure of the DUT. Eq. 1 gives the equivalent relation between IEC and TLP stress in terms of energy[8].

$$\text{Equivalent IEC energy(kV)} = \text{TLP current(A)} \cdot 1.3\text{(kV)} / 1.6\text{(A)}. \quad (1)$$

Moreover, the equivalent IEC stress can be calculated by Eq. 1 which stands for the upper limit of the protection ability. Apart from the united protection strategy of TVS and R_{iso} for the DUT in Fig. 2, this work uses another case to make a comparison where the protection strategy only includes R_{iso}. In two kinds

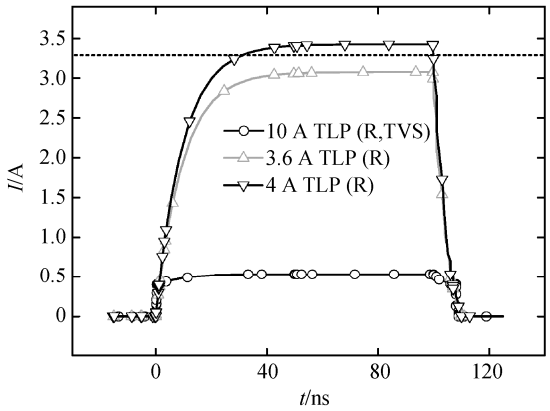

Fig. 5 Taking different TLP currents as the system input, the residual energy flowing into the DUT

of protection strategies, when taking different TLP currents as the system input, the situations that the residual energy flows into the DUT can be simulated as shown in Fig. 5. Specifically, in the only R strategy, the DUT is failed under 4-A TLP current (equivalent 3.25-kV IEC stress). Meanwhile, in R and TVS strategy, the DUT passes 10-A TLP current (equivalent 8.13-kV IEC stress) and 8 kV is the typical qualification goal prescribed in IEC 61000-4-2[9].

By contrast, this work also studies the residual energy flowing into the DUT with IEC stress as an input to show why this simulation method is not accurate enough. The system-level model in Fig. 6 is the same with the system-level model one in Fig. 2

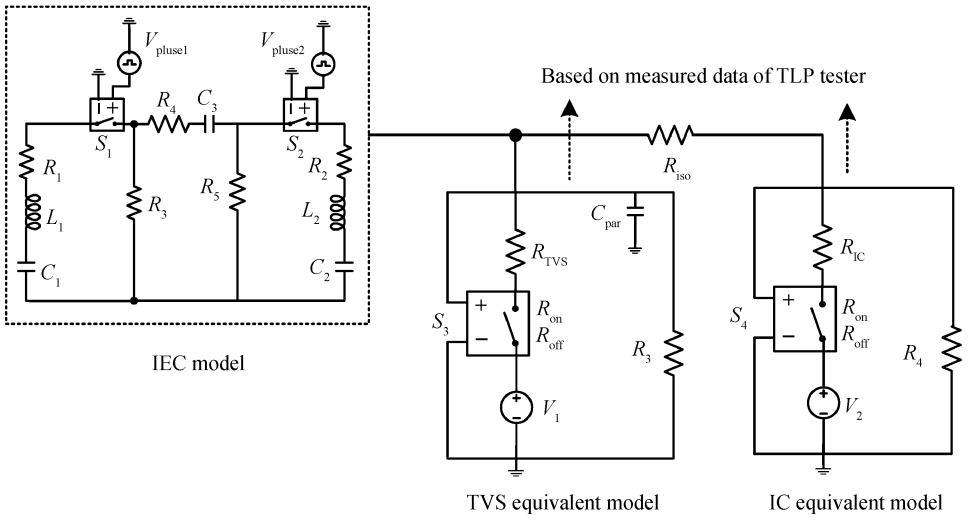

Fig. 6 Proposed circuit model with traditional IEC stress as an equivalent input of the IEC one

except for the input. The IEC model is used as an input which can deliver the standard double peak waveform prescribed in IEC 61000-4-2[1].

In the relevant two kinds of protection strategies, when taking IEC stress with different pre-charge voltages as the system input, the situations that the residual energy flows into the DUT can be simulated as shown in Fig. 7. It is can be seen that the transient currents flowing into the DUT are sine-like waves. However, the TLP stress is square wave. When the 3.3-A failure current under TLP stress is used as a failure standard of the sine-like waves in Fig. 7, it will bring the inaccuracy. Furthermore, Fig. 7 also shows the simulated predictive results. Specifically, in the only R strategy, the DUT is failed under 1.7-kV IEC stress. Meanwhile, in R and TVS strategy, the DUT passes 8-kV IEC qualification goal.

2 Experiment and Verification

In order to verify whether the system-level model has predictive ability with TLP input as equivalent IEC stress, this work manufactures the relevant printed circuit board (PCB) circuits. Taking R and TVS strategy as an example, the layout of the PCB is shown in Fig. 8. As for the failure standard, the pre and post *I–V* curves are compared to test whether the DUT is failed[10]. The step-size of ESD gun is 0.5 kV and the 30% skewing of the post *I–V* curve stands for the failure of the DUT. Fig. 9 shows the protection ability of two strategies for the DUT. Specifically, in the only R strategy, the DUT passes 2.5-kV IEC stress. Meanwhile, in both the R and TVS strategy, the DUT passes the typical qualification goal 8-kV IEC stress. Moreover, comparison results of the proposed and traditional method for predicting the failure of the DUT are shown in Table 1. The results illustrate that the proposed system-level circuit model with TLP input has more accurate prediction ability.

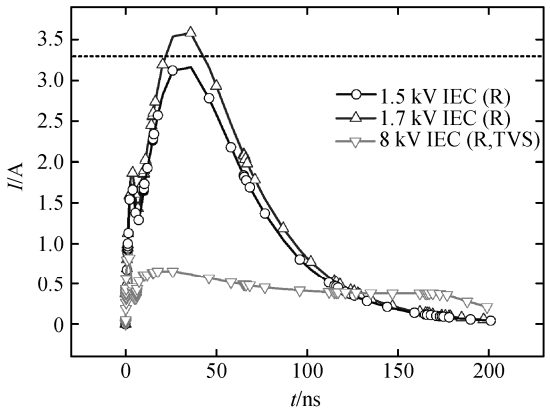

Fig. 7　Taking IEC stress with different pre-charge voltages as the system input, the residual energy flowing into the DUT

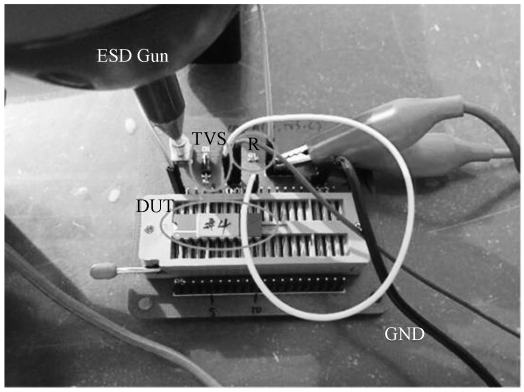

Fig. 8　Layout of PCB with the R and TVS protection strategy

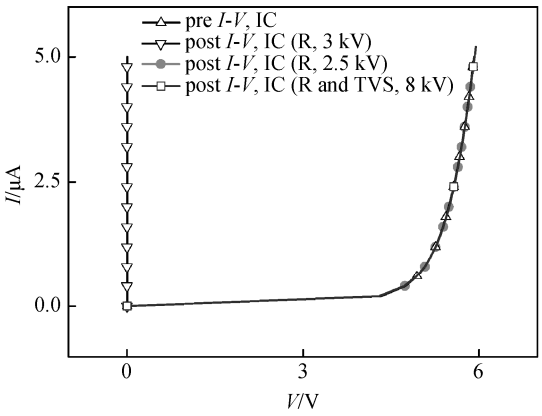

Fig. 9　Protection ability of two strategies for the DUT with the pre and post *I–V* test method

Table 1　Comparison results of the proposed and traditional method for predicting the failure of the DUT (kV)

Methods	R		R and TVS
	Pass	Failure	
Proposed simulated method	2.93	3.25	8.13
Traditional simulated method	1.50	1.70	8.00
Measurement	2.50	3.00	8.00

3 Conclusion

Although the protection elements such as TVS can filter the main energy of the IEC stress, there is still residual energy flowing into the DUT. Previous work uses the failure current I_{t2} of the DUT under TLP test as a system-level failure standard under the residual energy. As was mentioned before, this kind of equivalent method is not accurate. This work delivers a TLP stress into system-level protection models to analyze the performance of the circuits. The residual energy in this station is still a square wave like the TLP stress and it ensures that the failure standard under TLP test are applied to system-level accurately. Meanwhile, through the equivalent relation of the TLP and IEC stress, this kind of system-level analysis method predicted the ability of protection circuits for resisting the IEC stress. Finally, the verification results illustrate that the proposed system-level circuit model with the TLP input has more accurate prediction ability.

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