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A High-Resolution Analog Interface for Capacitive MEMS Gyroscope with Integrated SAR-ADC

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Abstract The authors present a drive and sense interface for MEMS vibratory gyroscopes. A gm-stage and a TIA are employed as the first stage to achieve low-noise C/V conversion. The signals of both drive mode and sense mode are converted to digital domain by integrated 1.25 MS/s 14-bit SAR-ADCs. With this strategy, the complexity of the analog circuit is reduced, and the signal in digital domain can be manipulated more accurately. The interface is applicable for the MEMS gyroscopes whose resonant frequency is from 3 kHz to 15 kHz. The circuit is designed in a 0.18 μm CMOS process. Experimental results show that the capacitive noise density of the output is achieved to 0.03 aF/√Hz at 3.5 kHz.

Key words capacitive interface circuit; MEMS gyroscope; SAR-ADC

一种集成 SAR-ADC 的电容式 MEMS 陀螺仪高精度模拟接口电路

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摘要 提出一种为MEMS振动陀螺仪设计的驱动和检测接口电路。第一步采用通用级和TIA得到低噪声C/V转换, 同时集成采样率 1.25 MS/s 的 14 位 SAR-ADCs, 将驱动和感应模式的信号转换到数字域。采用这种策略, 模拟电路的复杂性被降低, 数字域的信号可以更精确操作。此接口适用于共振频率为 3~15 kHz 的 MEMS 陀螺仪。此电路在 0.18 μm CMOS 工艺流片。实验结果显示, 在 3.5 kHz 频率下, 输出电容的噪声密度为 0.03 aF/√Hz。

关键词 电容接口电路; MEMS 陀螺仪; SAR-ADC
中图分类号 TN492

Micro-machined angular sensors have become an important part of electronic motion control systems in many applications like automotive, navigation and consumer electronics. Due to micromechanical manufacture technology, a lot of benefits can be obtained: smaller, lighter, and lower power consumption[1−2]. Typically, the readout circuits for sense mode of inertial sensors are open-loop. However, the capacitive variation of the gyroscope is extremely small, which is of the order of aF, high performance in terms of high resolution and low sensitivity to the temperature and process variation is demanded. Temperature has great influence on the sensor quality factor and process variation leads to quadrature errors inevitably. To solve these problems, a closed-loop readout interface is implemented in the sense mode. Since the feedback force against the variation suppress the movement, the dynamic range

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and the linearity of the system can be greatly improved as well.

In this paper, a drive and sense interface for MEMS (micro-electro-mechanical systems) gyroscope is presented. The system consists of two parts: analog domain and digital domain. Compared to the analog signal, digital signal has higher quality and easier manipulated. Capacitive variation of the gyroscope is sensed and amplified in analog domain, and then converted to digital signal by the integrated ADC (analog-to-digital converter). After the digital signals are processed in the FPGA (field- programmable gate array), integrated DAC (digital-to-analog converter) converts the signal back to analog signal and feedbacks to the gyroscope.

1 System Architecture

Fig. 1 shows the block diagram of the implemented gyroscope system. The gyroscope system requires two basic loops: the drive loop to actuate the gyroscope at the resonant frequency and the sense loop with amplifier and demodulation to obtain the rotation rate. According to the symmetrical structure of the vibratory gyroscope schematic, the two differential capacitive variation of the one axis is approximately equal. Then the basic model of the vibratory gyroscope can be represented by the two differential capacitors shown in the dashed box. Since gyroscopes requiring a high bias voltage for actuating oscillation, a 24 V voltage is applied to the mass.

The gyroscope is actuated at the resonant frequency of the drive mode along the *x*-axis (drive axis) with constant amplitude. According to the Coriolis Effect, the gyroscope responds to a rotation rate along the *z*-axis, resulting a vibration along *y*-axis (sense axis)[3]. The signal of the capacitive variation is sensed by a low-noise C/V (capacitance-to-voltage) conversion amplifier, consisting of a gm-stage and a TIA (trans-impendence amplifier), and then filtered by a high pass and a low pass filter. In order to maximize the use of output amplitude, an AGC (automatic gain control) is applied in the loop to adjust loop gain. Then the analog signal is transferred to digital domain by a SAR-ADC (successive approximation register analog-to-digital converter). Due to the resonant of the gyroscope is from 3 kHz to 15 kHz, a sample rate of 1.25 MS/s SAR-ADC is implemented for oversampling to achieve a higher resolution.

The oscillation of the gyroscope is controlled by a PLL (phase locked loop). The PLL tracks the resonant frequency of the drive mode, and feedbacks the gyroscope to ensure the sense mode oscillate at the same frequency. In this way, the maximum signal amplitude can be obtained by minimum energy cost[4−5]. The corresponding digital control loops are implemented on the FPGA, including filter, PID

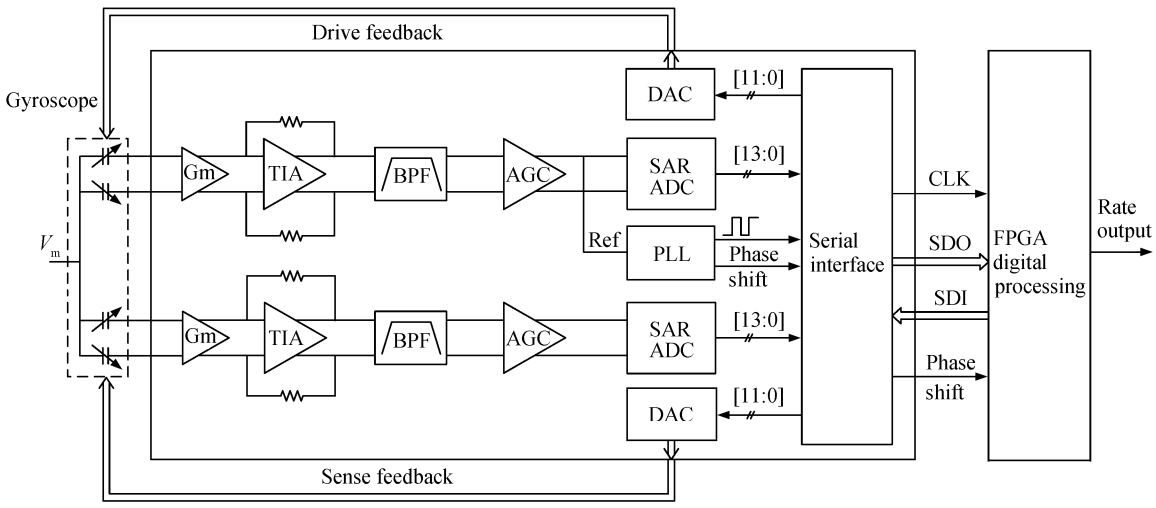

Fig. 1　System-level block diagram of the gyroscope

(proportional-integral-derivative) controller and rotation rate demodulation. Then the DAC received the digital results and feedback the electrostatic force to actuate the gyroscope. The feedback control can be implemented on the feedback electrode which is separated from the sense electrode[6−7]. A photograph of the fabricated gyroscope is shown in Fig. 2.

Phase shift of closed drive loop should be exactly 360°. However, external factors, such as temperature, have a large influence on the phase shift of analog blocks. So the phase shift of every stage is not allowed to be more than 1°. A maximum phase shift of ±5° generated by PLL is adequate to make the compensation.

This design mainly focuses on a high-resolution interface circuit design, thus low-noise performance is the major task. According to the system architecture, noise figure of the system is mainly determined by the first C/V conversion stage, while the noise of following stages is greatly suppressed by high gain of the conversion in closed loop[8]. So the C/V conversion design is crucial in this work.

2 Circuit Blocks

2.1 Charge sensitive amplifier

Fig. 3 shows the low-noise C/V conversion as the first stage of the interface. Common-drain PMOSs are employed to provide transconductance. The capacitors in the dashed box represent the differential sense capacitors of the gyroscope. Assuming the capacitive variation of ΔC can be expressed as

$$\Delta C_{\mathrm{s}} = \Delta C_{\mathrm{s,max}} \sin \omega_{\mathrm{r}} t, \tag{1}$$

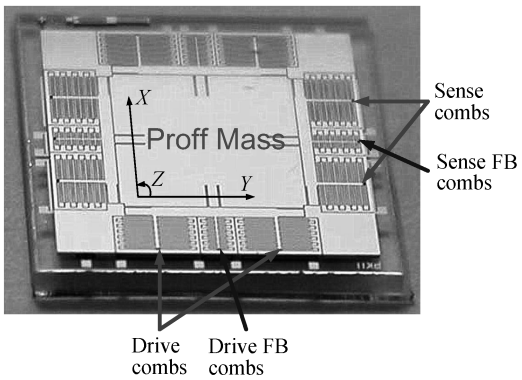

Fig. 2 Photograph of the fabricated gyroscope

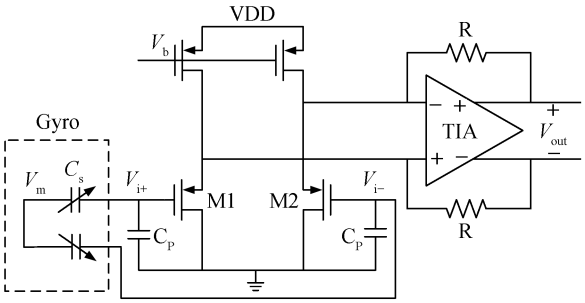

Fig. 3 C/V conversion

where $\Delta C_{\mathrm{s,max}}$ is the maximum variation of C_{s}, ω_{r} is the resonant frequency of the drive mode. Due to charge conservation, the input can be described as

$$V_{\mathrm{i}} = V_{\mathrm{i+}} - V_{\mathrm{i-}} = \frac{\Delta C_{\mathrm{s0}} \cdot V_{\mathrm{m}}}{C_{\mathrm{s0}} + C_{\mathrm{p}}} \cdot \sin \omega t, \tag{2}$$

where V_{m} is the high voltage applied on the mass of gyroscope. So the output of TIA can be expressed as

$$V_{\mathrm{out}} = g_{\mathrm{m}} R \cdot \frac{\Delta C_{\mathrm{s0}} \cdot V_{\mathrm{m}}}{C_{\mathrm{s0}} + C_{\mathrm{p}}} \cdot \sin \omega t\,. \tag{3}$$

V_{m} is related to the gain of the conversion, which means that V_{m} needs to be as large as possible. In this work, V_{m} is set to 24 V.

The noise of the conversion is mainly determined by the M1, M2 and the operational amplifier of the TIA. In order to achieve a low-noise performance, a PMOS input fully-differential 2-stage operational amplifier is employed, and the sizes of the transistors are optimized. The simulation results show that the equivalent input referred noise of the conversion stage is 16.2 nV/√Hz at 10 kHz.

2.2 Band pass filter

The band pass filter is composed of a 1-order HPF (high pass filter) and a 2-order LPF (low pass filter). The schematic is shown in Fig. 4.

The cut-off frequency of the high pass and low pass can be given as follows:

$$f_{\mathrm{H}} = \frac{1}{2\pi R_1 C_2}, \tag{4}$$

$$f_{\mathrm{L}} = \frac{1}{2\pi\sqrt{R_2 R_3 C_3 C_4}}. \tag{5}$$

As mentioned in Section 1, the variation of the phase

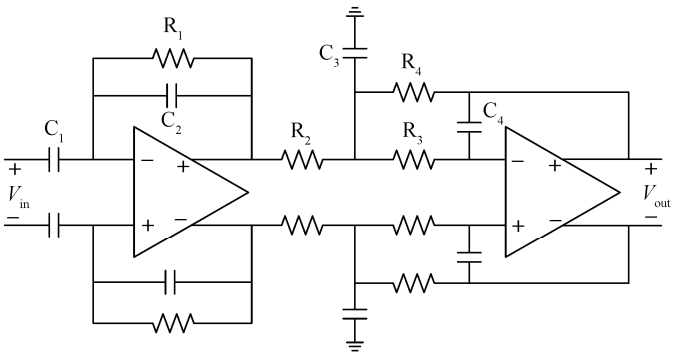

Fig. 4　Band pass filter

shift influenced by external factors in the analog circuit needs to be decreased to the level that phase shift signal generated by PLL can compensate for, which is ±5º. Supposing the absolute phase shift is decreased, the relative variation of phase shift will be suppressed correspondingly. Thus, the phase shift at the resonant frequency of each filter is set to less than 1º.

However, the phase shift of a typical 2-order LPF can be more than 10º, which greatly exceeds the design requirement. In this work, a high-Q low pass filter is adopted to obtain a small phase shift at the resonant frequency of the gyroscope. The quality factor of the LPF is given in Eq. (6):

$$Q_{\mathrm{L}} = \frac{\sqrt{C_3/C_4}}{\sqrt{R_3R_4/R_2^2}+\sqrt{R_3/R_4}+\sqrt{R_4/R_3}}. \qquad (6)$$

At the meantime, a resonant peak will appear at the center frequency f_{L} of the LPF in the spectrum, which may result in a worsening of noise performance. In order to solve this problem, a digital filter is applied in the FPGA software algorithm to suppress the signal at the frequency of f_{L}.

2.3　SAR-ADC

The SAR-ADC provides high resolution at medium speed, which is easy to integrate in CMOS technology[5]. In this application, both drive mode and sense mode are working in the closed-loop fashion. Therefore, the monotonicity is highly required, while INL and DNL are not so important. A 1.25 MS/s 14-bit SAR-ADC is designed in this work, based on 2-stage DAC architecture, that 7-bit R-DAC is used for MSB and 7-bit C-DAC for LSB. The fully differential architecture is shown in Fig. 5.

The schematic of the fully differential comparator is illustrated in Fig. 6. Two-stage pre-amplifier and a latch are cross connected to achieve high speed and high gain. Because the offset of the comparator has a great influence to the monotonicity of the conversion, offset cancellation is introduced in this design, performing at the output of the first pre-amplifier stage also the input of the second pre-amplifier. The simulation results show that compare time is less than 3 ns.

During sampling phase, all bottom plates of the capacitors are connected to the differential inputs, and all top plates are connected to a reference voltage V_{cm}, while the comparator performs offset cancellation. Because all capacitors are connected together to be the maximum, the sampling phase occupies two clock cycles. During conversion phase, the bottom plates are switched between the high and low reference voltages, and the comparator results determine the current bit.

A Verilog-A varactor model is employed to achieve a sinusoidal fashion variation of the sense capacitors. Additionally, a 12-bit DAC simulator is used to observe and analyze the ADC outputs. The input voltage signal is at 10 kHz, and the sample rate of the SAR-ADC is 1.25 MS/s. Fig. 7 shows the output signal of the DAC when the sense capacitance varies by 10 fF. The spectrum of the analog output is illustrated in Fig. 8.

2.4　PLL

An internal PLL, shown in Fig. 9, is used to

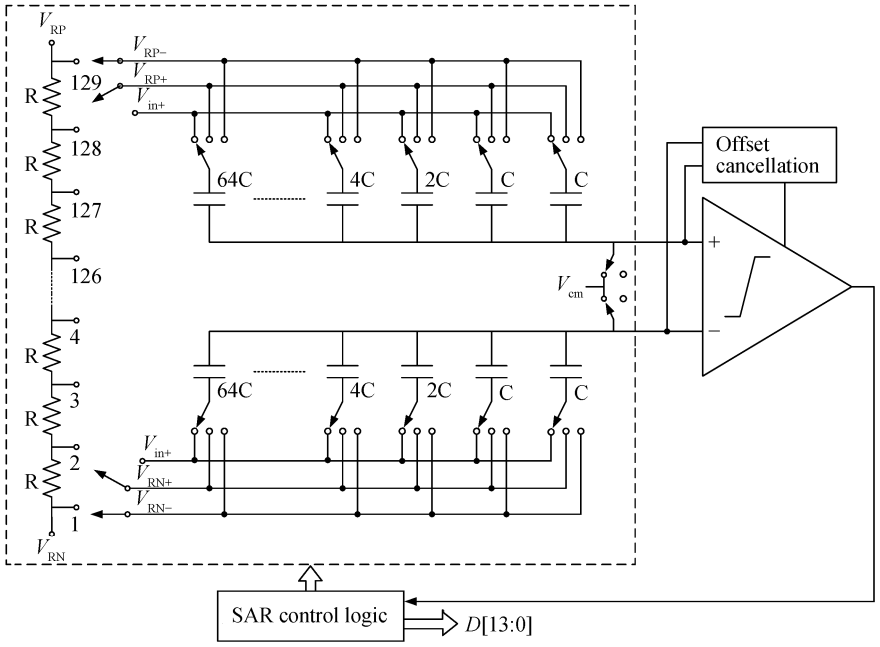

Fig. 5 Schematic of the implemented 14-bit SAR-ADC

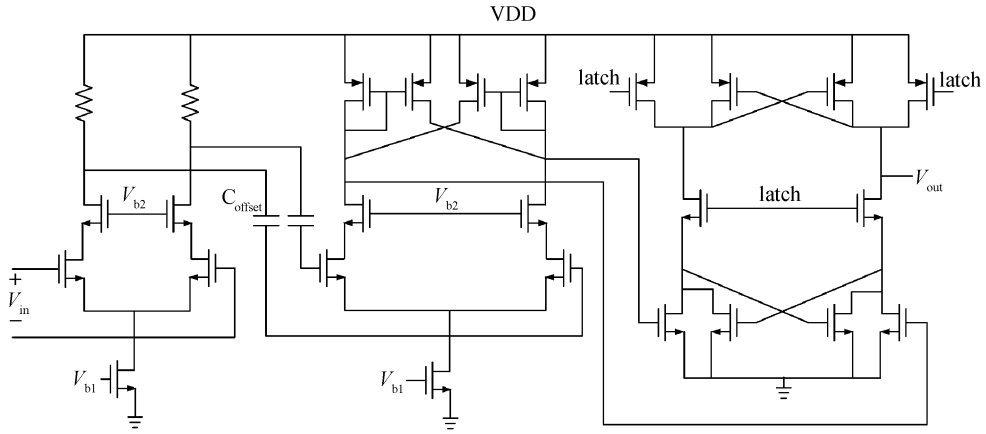

Fig. 6 Schematic of the comparator

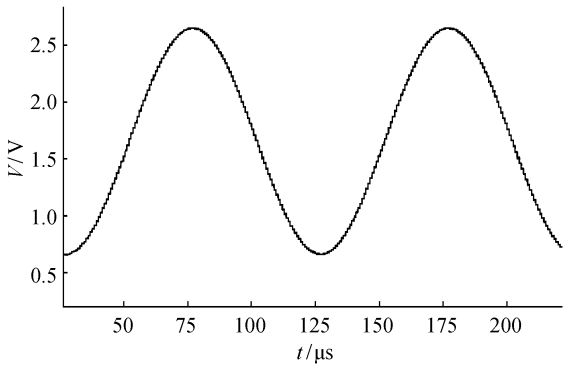

Fig. 7 Output signal of the DAC simulator

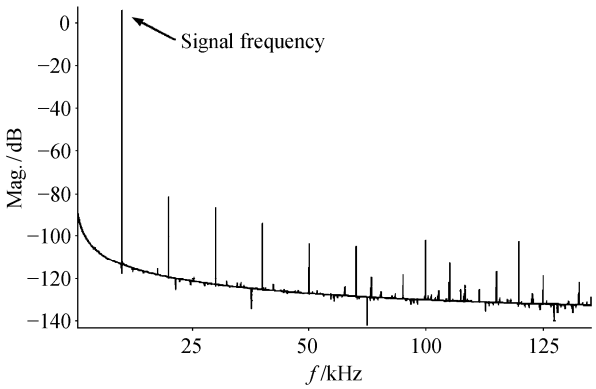

Fig. 8 Output signal spectrum

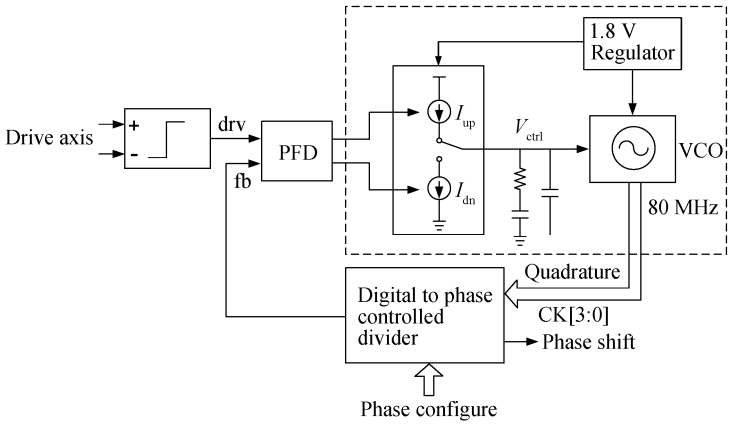

Fig. 9　Topology of the PLL

generate an 80 MHz clock signal for the chip, which is a configurable frequency multiplication of the resonant frequency of the drive mode. The multi-modulus prescalers, which are capable of frequency division over a large, contiguous range, are used in the divider. The asynchronous divider is based on the 2/3 stage machines. By maintaining an asynchronous counting method, the speed is faster and the power dissipation is largely reduced. Moreover, a phase adjustable signal at the resonant frequency of the drive mode is generated by the PLL. Due to the quadrature outputs of the oscillator, the minimum step of the phase shifter is 3.125 ns.

3　Experimental Results

The drive and sense interface circuit has been implemented using 0.18 μm CMOS process. The chip area is 3 mm×1.8 mm. A microphotograph of the chip is shown in Fig. 10.

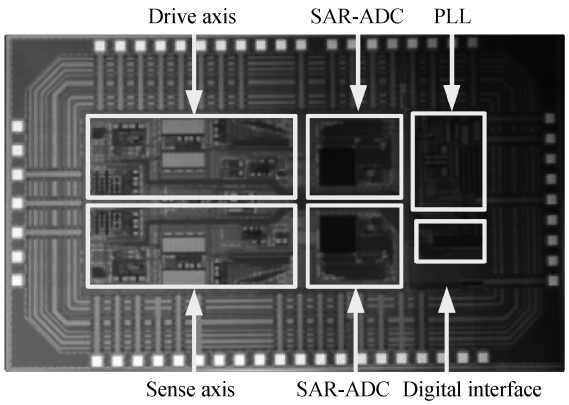

Fig. 10　Microphotograph of the chip

The ASIC has been tested with two kinds of MEMS gyroscopes, whose resonant frequencies are 3.47 kHz and 7.81 kHz. The analog outputs before the ADC are both illustrated in Fig. 11. In each figure, the top two signals are the differential outputs of the sense axis, and the bottom two signals are the difference result of the outputs and the electrostatic force applied on the gyroscopes. As shown in the figure, the output of the readout lags behind the electrostatic force by 90° phase shift.

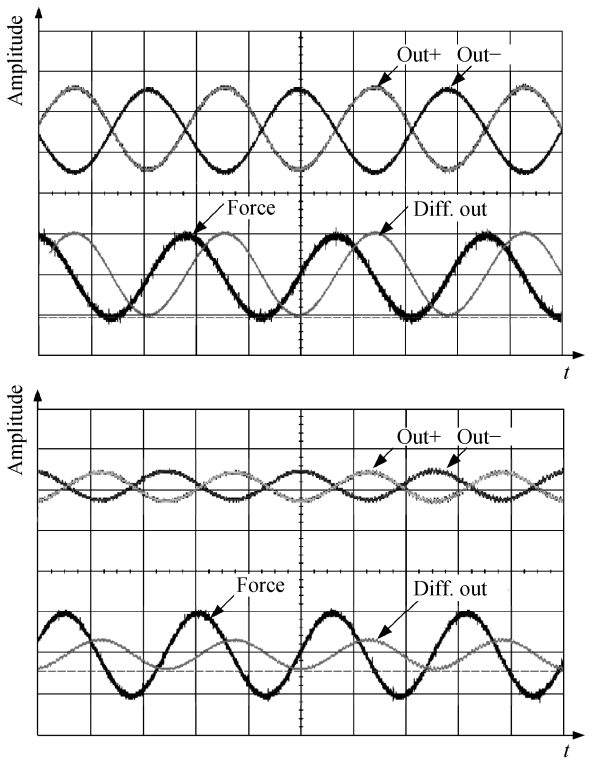

Fig. 11　Outputs of the analog readouts

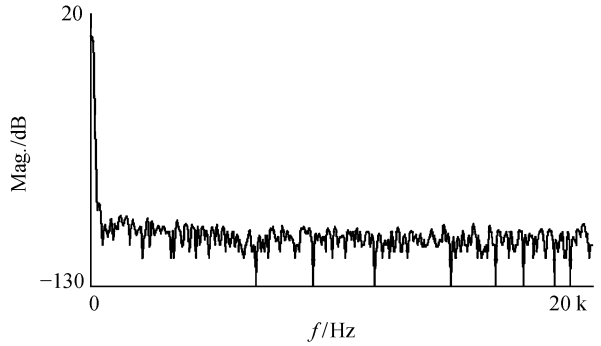

Fig. 12 Spectrum of the output

Table 1 Parameters of the interface

Parameter	Value
Resonant frequency	3–15 kHz
C/V conversion gain	0.55 V/fF
capacitive noise density	0.03 aF/√Hz
Sample rate of ADC	1.25 MS/s
Power supply	3.3 V
Supply voltage on mass	24 V
Power consumption (chip)	22.6 mW

The spectrum of the output is shown in Fig. 12. The common voltage of the signal is 1.65 V. The measured noise density is 16.6 μV/√Hz at 3.5 kHz. According to the C/V conversion gain of 0.55 V/fF, the capacitive noise density is 0.03 aF/√Hz. The main parameters of the interface is shown in Table 1.

4 Conclusion

A fully differential low-noise high-resolution interface circuit for MEMS capacitive gyroscope is presented. The interface is composed of a charge-voltage transfer front-end, a PLL, DACs, and SAR-ADCs. The integration of the SAR-ADCs is very suited for this application to improve noise performance. The gyroscope and the chip can be bonded in one package, directly connected to the digital signal processing FPGA. The interface circuit is designed in a 0.18 μm CMOS process. The experimental results show that capacitive noise density of the output is 0.03 aF/√Hz at 3.5 kHz.

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